AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph on page 15, lines 5-14 as follows:

Figure 9 illustrates an exemplary implementation of the loop voltage amplifier 802. The purpose of this amplifier is to amplify the error signal 810 so that it is less constrained by the matching and noise requirements of the subsequent circuitry in the modulator. The error signal 810 is inversely proportional to the VCO gain. Assuming a maximum VCO gain of 60 MHz/V and an average frequency deviation of 60 Hz, the signal level at the VCO input will be about 1 mV. Assuming further that the maximum residual error is about 5 percent, the minimum level for the error signal ~~310~~ 810 will be about 50 μV. Since the loop voltage may vary by as much as 2V, depending on the transmitter output frequency and parameters spread, the dynamic range requirement of the modulator becomes greater than 90dB (20log(2V/50μV) = 92dB).

Please amend the paragraph on page 19, lines 5-7 as follows:

Figure 12 illustrates an exemplary implementation of the limit/delay block 804. In this figure, Q18, Q19, R18, and ~~R19~~ R20 provide the limiter, and the RC combination R18, R20, and C1, C2 provide the delay. The bias point is set by Q17 and R15.

Please amend the paragraph on page 19, lines 8-13 as follows:

Figure 13 illustrates an exemplary implementation of the mixer 806. In this figure, Q6-Q9 provide a standard Gilbert mixer, and R1 and R2 are the mixer load resistors. Q22 and Q23 (DC biased by ~~Q23~~ Q24, Q26 and R9, R11) are used for DC level shifting. The transconductance driving the integrating capacitor C1 is formed by Q3, Q4, Q10, and Q11 (DC biased by Q25 and R0). The voltage across C1 then controls the gain of the frequency path.